

PATENT APPLICATION

FORM PTO-1449	ATTY. DOCKET NO. 10008005	SERIAL NO.
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	APPLICANT Padmanabha Venkitakrishnan	
(Use several sheets if necessary)	FILING DATE 07/31/01	GROUP

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

RJ
"WATTCHE: A FRAMEWORK FOR ARCHITECT-LEVEL POWER ANALYSIS AND
OPTIMIZATIONS", Brooks et al., Proceedings of the 27th International
Symposium on Computer Architecture, June 2000, Vancouver, BC,
Pages 83-94

EXAMINER

EXAMINER

DATE CONSIDERED

3/16/05

PATENT APPLICATION

Sheet 1 of 1



FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR
APPLICANT'S INFORMATION DISCLOSURE
STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO. 10008005-1	APPLICATION NO. 09/920,382	CONFIRMATION NO.
APPLICANT Padmanabha Venkitakrishnan		
FILING DATE 07/31/2001	GROUP	

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
1A					
1B					
1C					
1D					
1E					
1F					
1G					
1H					
1I					
1J					
1K					

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	TRANSLATION
							YES
	1L						
	1M						
	1N						
	1O						
	1P						

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

<i>RJ</i>	1Q	Dake Liu and Christer Svensson - "Power Consumption Estimation in CMOS VLSI Chips" - June 1994- pages 663-670
<i>RJ</i>	1R	Rita Yu Chen, Mary Jane Irwin and Raminder S. Bajwa - "An Architectural Level Power Estimator" June 1998 - pages 1-5
	1S	

EXAMINER <i>Russ Smith</i>	DATE CONSIDERED 3/16/05
-------------------------------	----------------------------